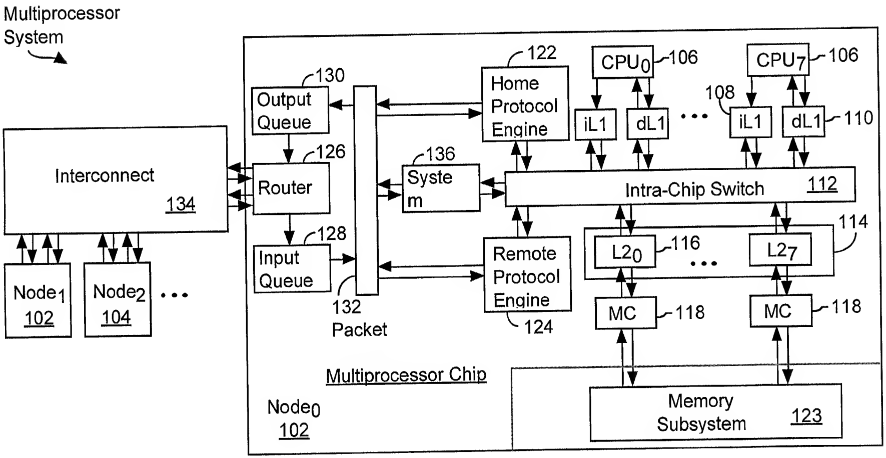

Multiprocessor System
Interconnect 134
Node1 102
Node2 104
Output Queue 130
Router 126
Input Queue 128
132 Packet
Syste m 136
Home Protocol Engine 122
Remote Protocol Engine 124
CPU0 106
CPU7 106
iL1
dL1
108
110
Intra-Chip Switch 112
114
L20 116
L27
MC 118
MC 118
Memory Subsystem 123
Multiprocessor Chip
Node0 102

Figure 1

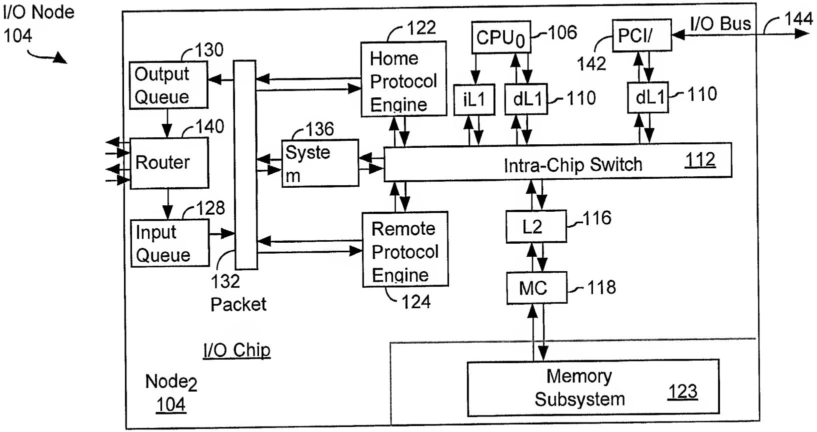

I/O Node
104
Output Queue
130
Router
140
Input Queue
128
132
Packet
Syste m
136
Home Protocol Engine
122
Remote Protocol Engine
124
CPU$_0$
106
iL1
dL1
110
PCI/
142
I/O Bus
144
dL1
110
Intra-Chip Switch
112
L2
116
MC
118
Memory Subsystem
123
I/O Chip
Node2
104

Figure 2

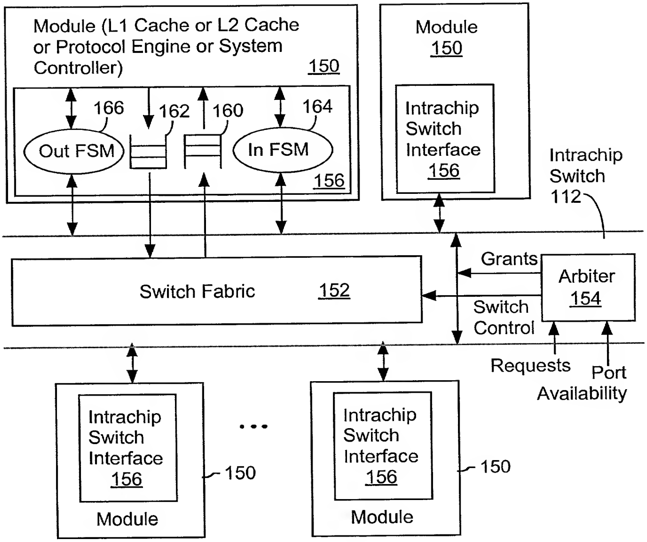
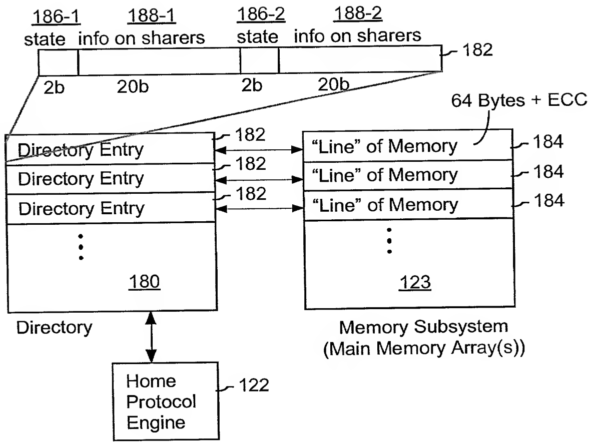

Module (L1 Cache or L2 Cache or Protocol Engine or System Controller)
150
166
162
160
164
Out FSM
In FSM
156
Module
150
Intrachip Switch Interface
156
Intrachip Switch
112
Grants
Arbiter
154
Switch Fabric
152
Switch Control
Requests
Port Availability
Intrachip Switch Interface
156
Module
150
• • •
Intrachip Switch Interface
156
Module
150

Figure 3



Directory State	Description
invalid	no remote copies
exclusive	exclusive remote copy
shared	one or more shared remote copies (limited pointer)
shared-cv	one or more shared remote copies (coarse pointer)

Node to Bit and Bit to Node AssignmentTable
(for sharer information field 188, coarse vector format)
189

	0	1	2	3	4	5	...		...	35	36	37	38	39
0	[0]	1	2	3	4	...		...	34	35	36	37	38	39
1	40	41	42	43	...		...	73	74	75	76		-	

Figure 4

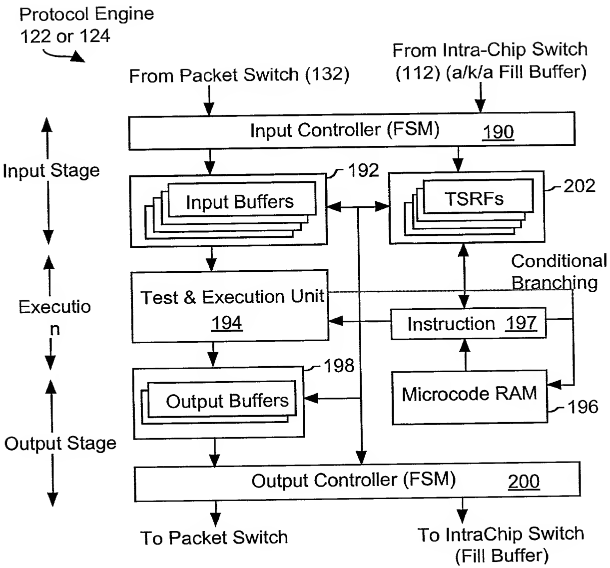


Figure 5

3b	4b	4b	10b
op	arg1	arg2	next PC

Microcode Instruction Format

Figure 6A

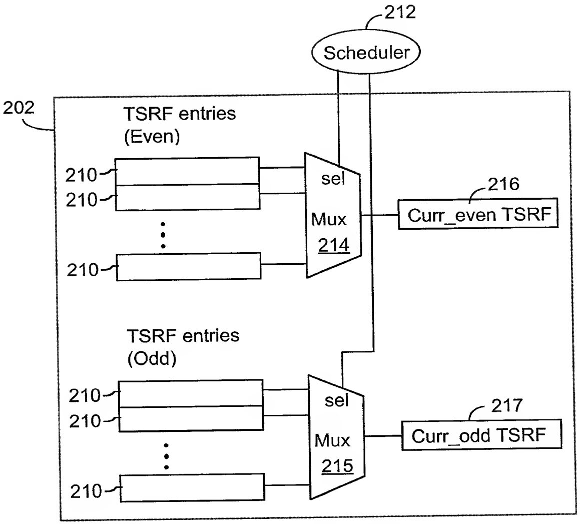
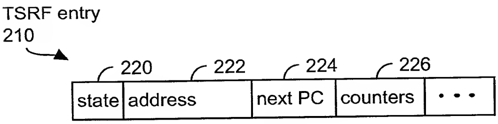
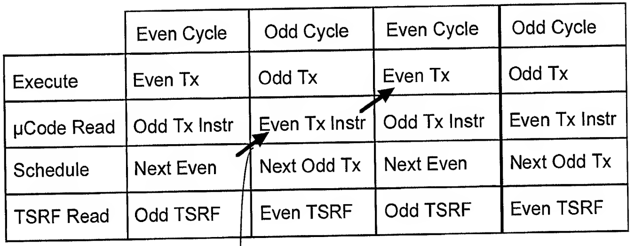


Figure 6B



TSRF entry format

Figure 6C



	Even Cycle	Odd Cycle	Even Cycle	Odd Cycle
Execute	Even Tx	Odd Tx	Even Tx	Odd Tx
µCode Read	Odd Tx Instr	Even Tx Instr	Odd Tx Instr	Even Tx Instr
Schedule	Next Even	Next Odd Tx	Next Even	Next Odd Tx
TSRF Read	Odd TSRF	Even TSRF	Odd TSRF	Even TSRF

Incorporate condition codes into determination of next PC for µCode Read

Figure 7A

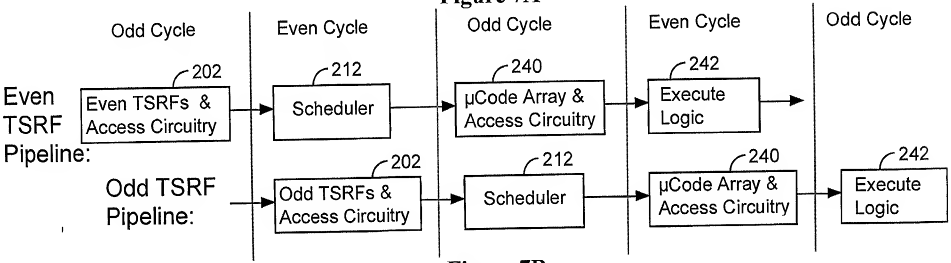


Figure 7B

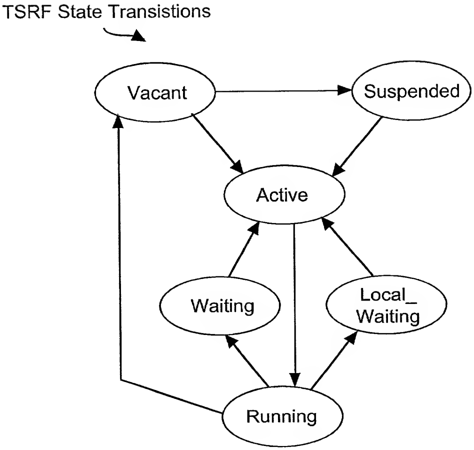

TSRF State Transistions
Vacant
Suspended
Active
Waiting
Local_ Waiting
Running

Figure 7C

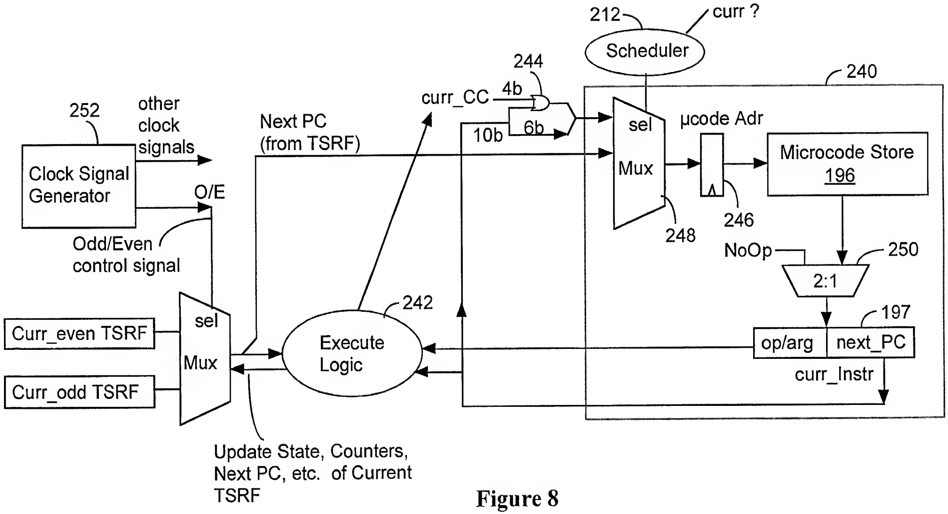
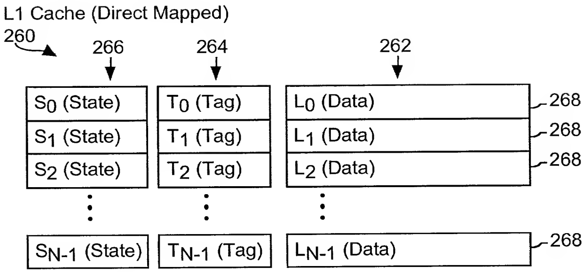
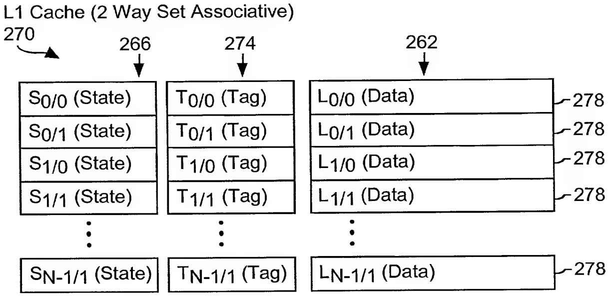

212
curr ?
Scheduler
240
244
curr_CC
4b
6b
10b
252
other clock signals
Clock Signal Generator
O/E
Odd/Even control signal
Next PC (from TSRF)
sel
Mux
µcode Adr
Microcode Store 196
246
248
NoOp
250
2:1
197
op/arg
next_PC
curr_Instr
242
Execute Logic
Curr_even TSRF
Curr_odd TSRF
sel
Mux
Update State, Counters, Next PC, etc. of Current TSRF

Figure 8



For Direct Mapped L1 Cache:
Address Bit Groups = ABCD
Line Address = ABC
Tag = A
Cache Index for Line = BC
State = invalid, shared, clean exclusive, dirty exclusive

Figure 9A



For 2-way Set Associative Cache:
Address Bit Groups = ABCD
Line Address = ABC
Tag = AB
Cache Index for Line = C

Figure 9B

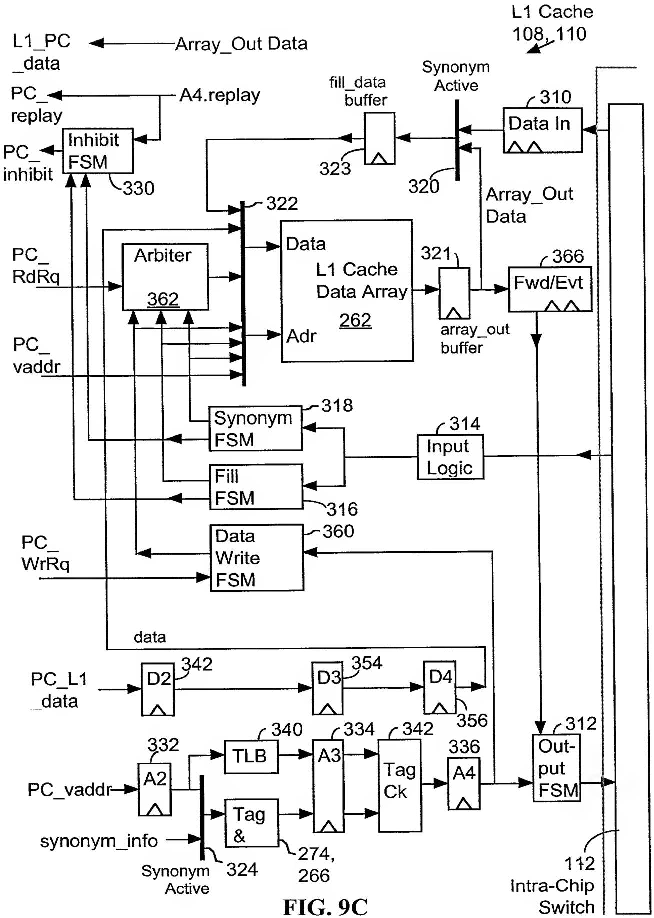

L1 Cache
108, 110
L1_PC
_data
Array_Out Data
PC_
replay
A4.replay
PC_
inhibit
Inhibit
FSM
330
fill_data
buffer
323
Synonym
Active
320
310
Data In
322
Array_Out
Data
PC_
RdRq
Arbiter
362
Data
L1 Cache
Data Array
262
Adr
321
array_out
buffer
366
Fwd/Evt
PC_
vaddr
318
Synonym
FSM
314
Input
Logic
Fill
FSM
316
360
PC_
WrRq
Data
Write
FSM
data
PC_L1
_data
D2
342
D3
354
D4
356
340
334
342
TLB
A3
Tag
Ck
332
A2
336
A4
312
Out-
put
FSM
PC_vaddr
Tag
&
274,
266
synonym_info
Synonym
Active
324
112
Intra-Chip
Switch

FIG. 9C

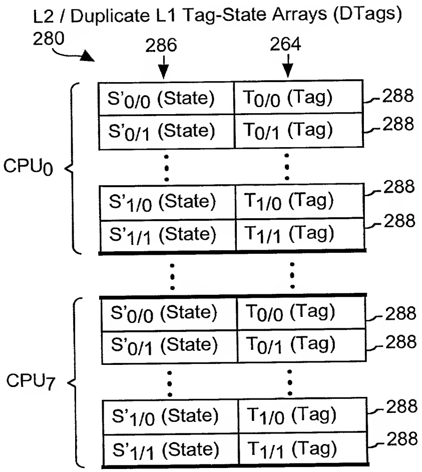


Figure 10A

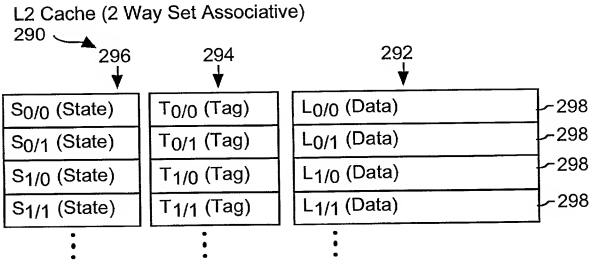


Figure 10B

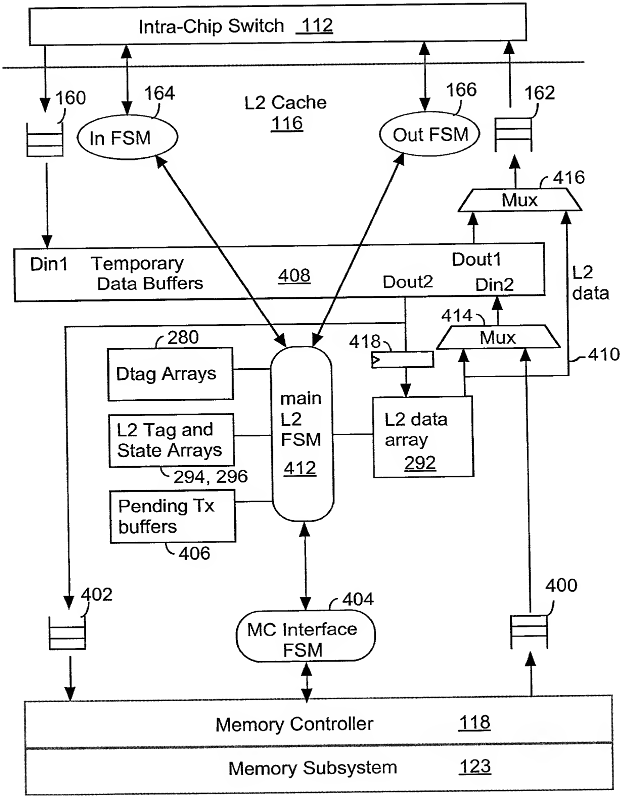

Intra-Chip Switch 112
L2 Cache
116
160
164
166
162
In FSM
Out FSM
416
Mux
Din1
Temporary
Data Buffers
408
Dout1
Dout2
Din2
L2
data
414
Mux
410
280
418
Dtag Arrays
main
L2
FSM
412
L2 data
array
292
L2 Tag and
State Arrays
294, 296
Pending Tx
buffers
406
402
404
400
MC Interface
FSM
Memory Controller
118
Memory Subsystem
123

FIG. 10C

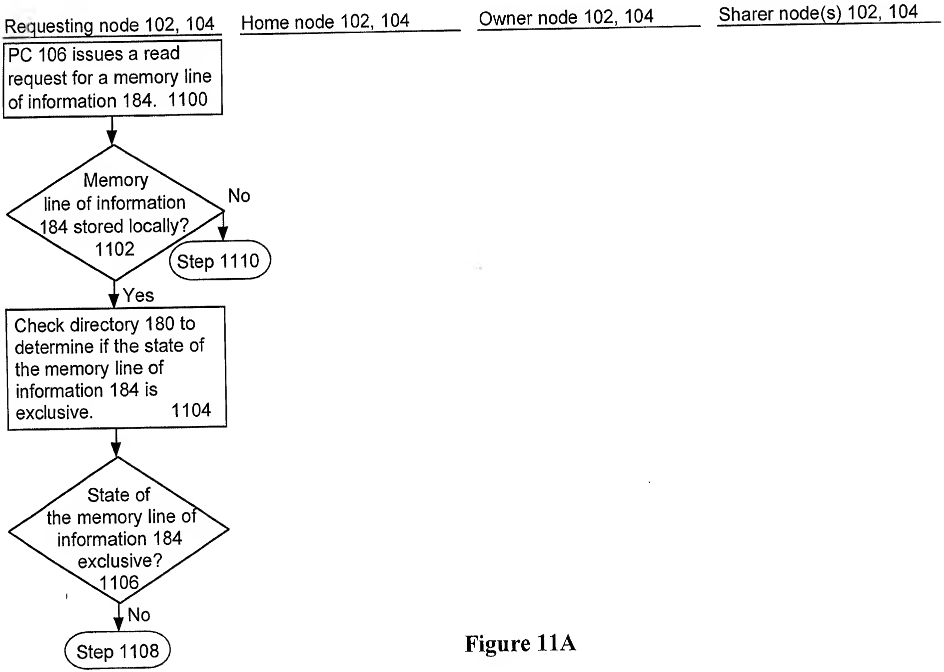

Requesting node 102, 104
Home node 102, 104
Owner node 102, 104
Sharer node(s) 102, 104
PC 106 issues a read request for a memory line of information 184. 1100
Memory line of information 184 stored locally? 1102
No
Step 1110
Yes
Check directory 180 to determine if the state of the memory line of information 184 is exclusive. 1104
State of the memory line of information 184 exclusive? 1106
No
Step 1108

Figure 11A

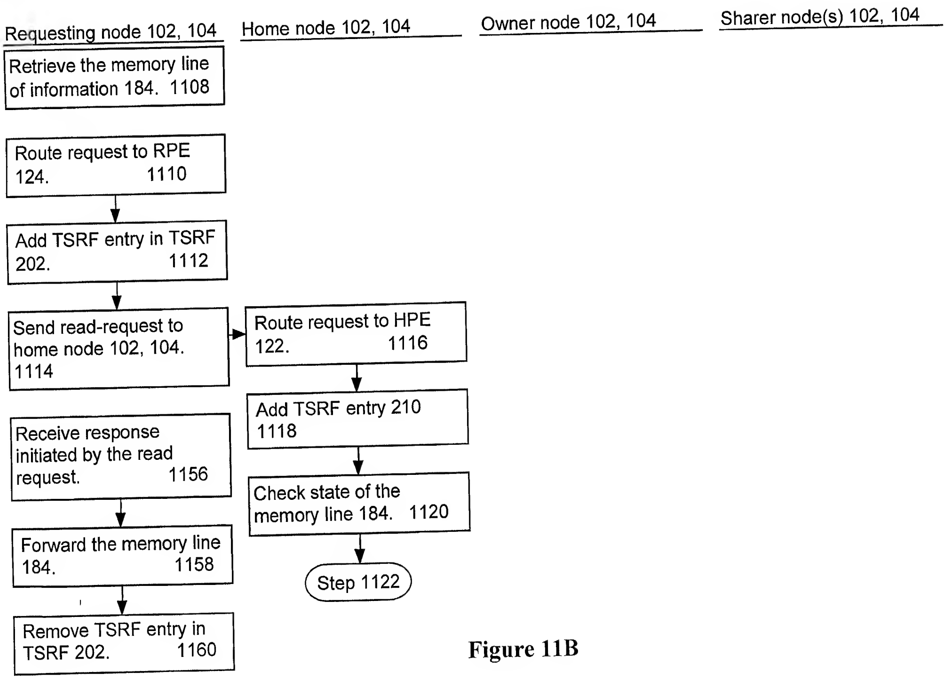

Requesting node 102, 104
Home node 102, 104
Owner node 102, 104
Sharer node(s) 102, 104
Retrieve the memory line of information 184. 1108
Route request to RPE 124. 1110
Add TSRF entry in TSRF 202. 1112
Send read-request to home node 102, 104. 1114
Route request to HPE 122. 1116
Add TSRF entry 210 1118
Check state of the memory line 184. 1120
Step 1122
Receive response initiated by the read request. 1156
Forward the memory line 184. 1158
Remove TSRF entry in TSRF 202. 1160

Figure 11B

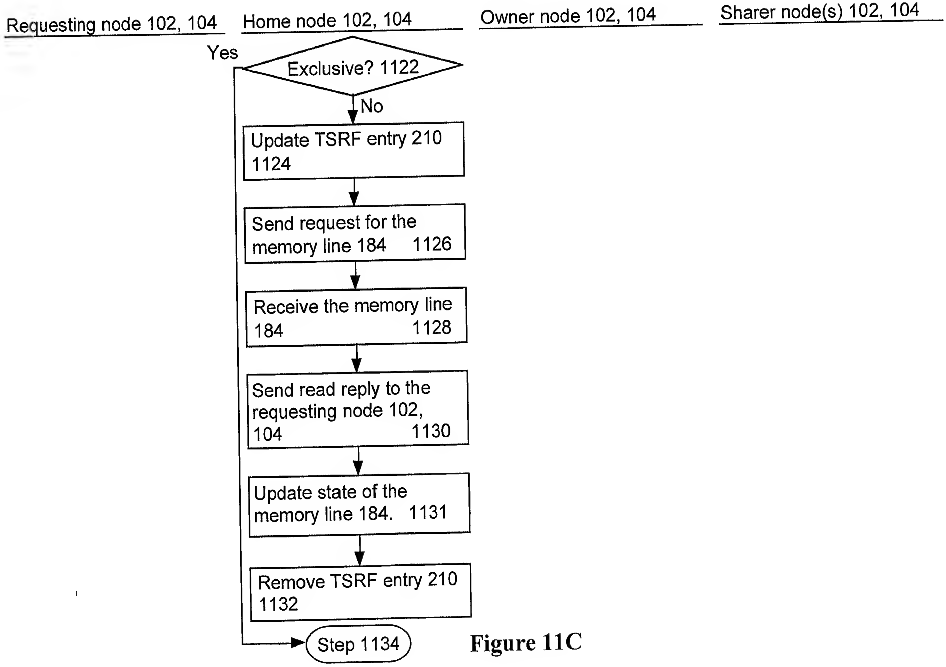

Requesting node 102, 104
Home node 102, 104
Owner node 102, 104
Sharer node(s) 102, 104
Exclusive? 1122
Yes
No
Update TSRF entry 210 1124
Send request for the memory line 184 1126
Receive the memory line 184 1128
Send read reply to the requesting node 102, 104 1130
Update state of the memory line 184. 1131
Remove TSRF entry 210 1132
Step 1134

Figure 11C

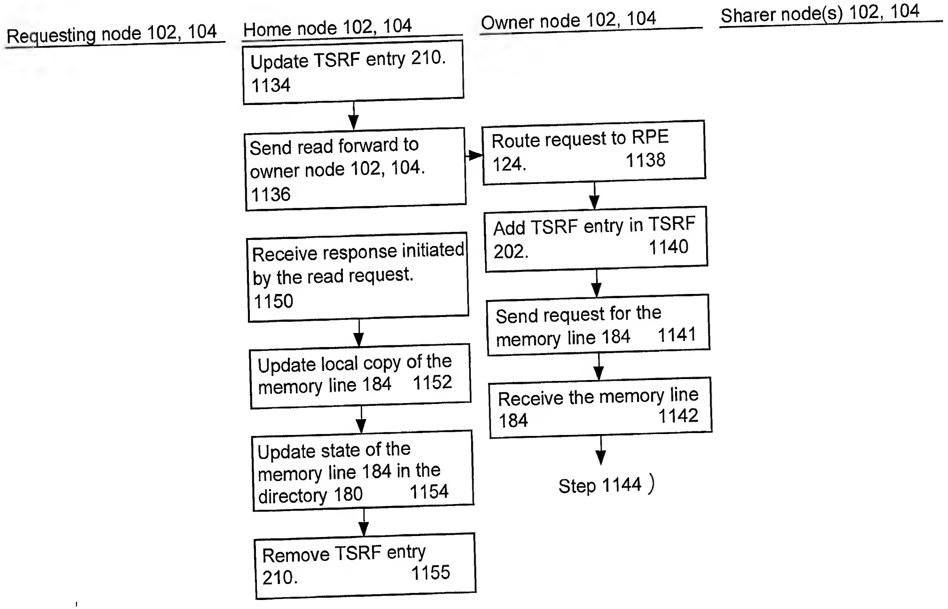

Requesting node 102, 104
Home node 102, 104
Owner node 102, 104
Sharer node(s) 102, 104
Update TSRF entry 210. 1134
Send read forward to owner node 102, 104. 1136
Route request to RPE 124. 1138
Add TSRF entry in TSRF 202. 1140
Send request for the memory line 184 1141
Receive the memory line 184 1142
Step 1144)
Receive response initiated by the read request. 1150
Update local copy of the memory line 184 1152
Update state of the memory line 184 in the directory 180 1154
Remove TSRF entry 210. 1155

Figure 11D

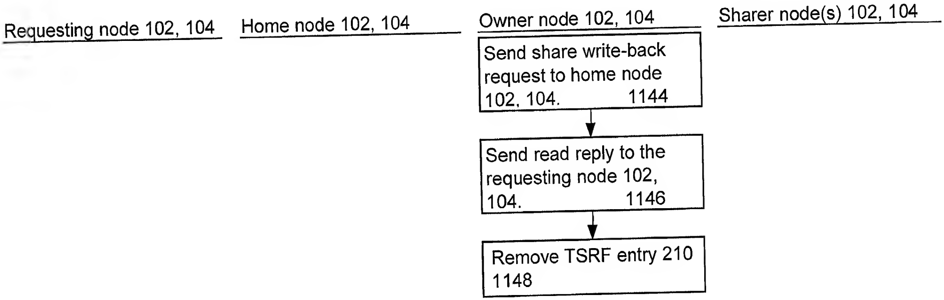

Requesting node 102, 104
Home node 102, 104
Owner node 102, 104
Sharer node(s) 102, 104
Send share write-back request to home node 102, 104. 1144
Send read reply to the requesting node 102, 104. 1146
Remove TSRF entry 210 1148

Figure 11E

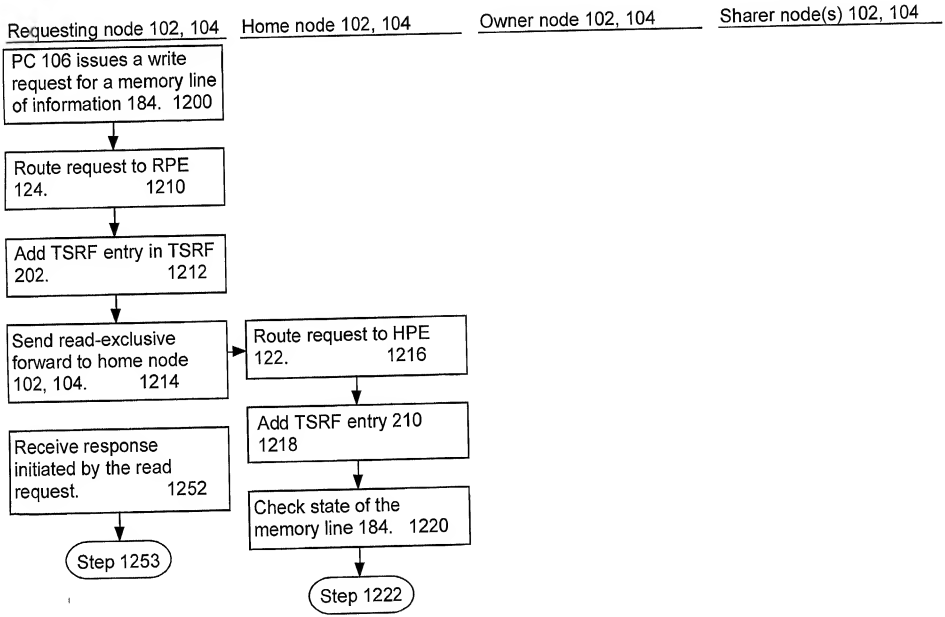

Requesting node 102, 104
Home node 102, 104
Owner node 102, 104
Sharer node(s) 102, 104
PC 106 issues a write request for a memory line of information 184. 1200
Route request to RPE 124. 1210
Add TSRF entry in TSRF 202. 1212
Send read-exclusive forward to home node 102, 104. 1214
Route request to HPE 122. 1216
Add TSRF entry 210 1218
Check state of the memory line 184. 1220
Step 1222
Receive response initiated by the read request. 1252
Step 1253

Figure 12A

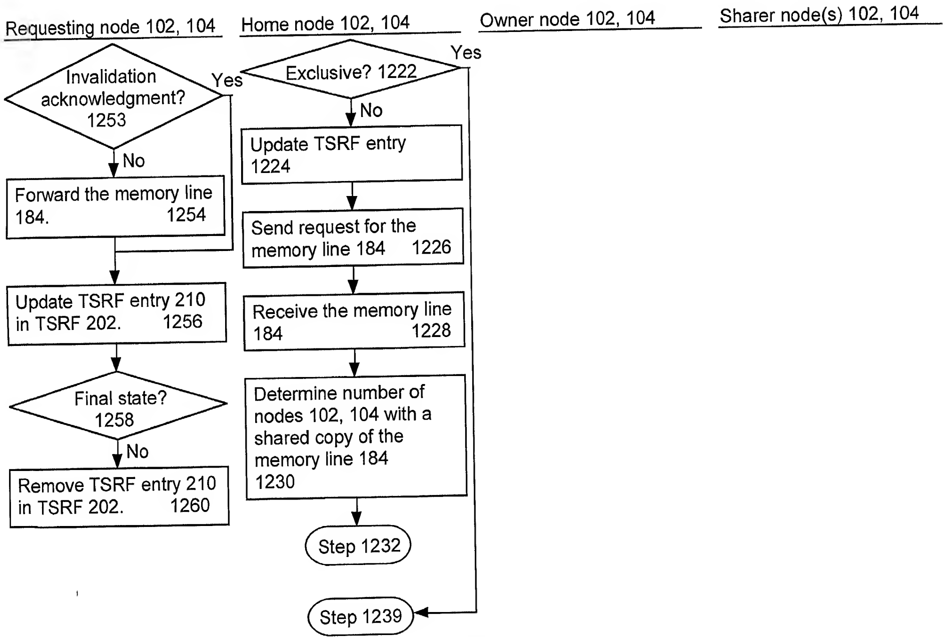

Requesting node 102, 104
Home node 102, 104
Owner node 102, 104
Sharer node(s) 102, 104
Invalidation acknowledgment? 1253
Yes
No
Forward the memory line 184. 1254
Update TSRF entry 210 in TSRF 202. 1256
Final state? 1258
No
Remove TSRF entry 210 in TSRF 202. 1260
Exclusive? 1222
Yes
No
Update TSRF entry 1224
Send request for the memory line 184 1226
Receive the memory line 184 1228
Determine number of nodes 102, 104 with a shared copy of the memory line 184 1230
Step 1232
Step 1239

Figure 12B

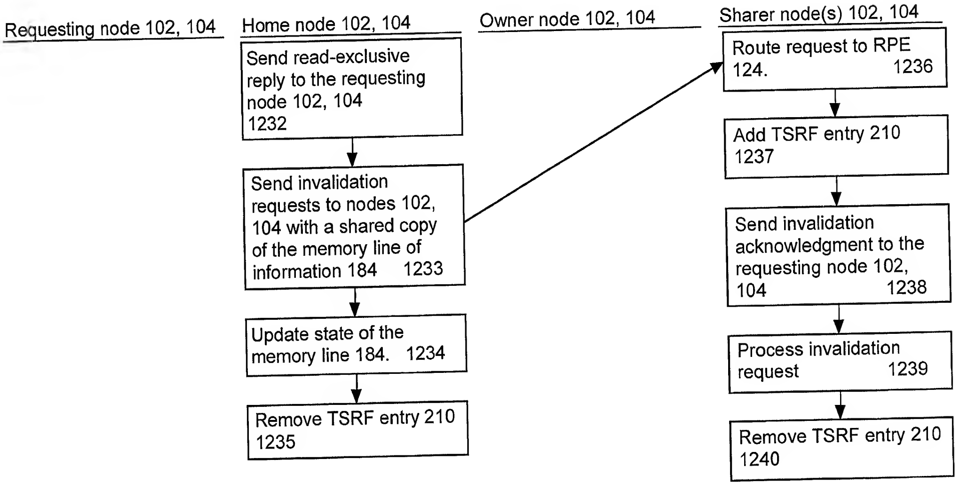

Requesting node 102, 104
Home node 102, 104
Owner node 102, 104
Sharer node(s) 102, 104
Send read-exclusive reply to the requesting node 102, 104
1232
Send invalidation requests to nodes 102, 104 with a shared copy of the memory line of information 184
1233
Update state of the memory line 184.
1234
Remove TSRF entry 210
1235
Route request to RPE 124.
1236
Add TSRF entry 210
1237
Send invalidation acknowledgment to the requesting node 102, 104
1238
Process invalidation request
1239
Remove TSRF entry 210
1240

Figure 12C

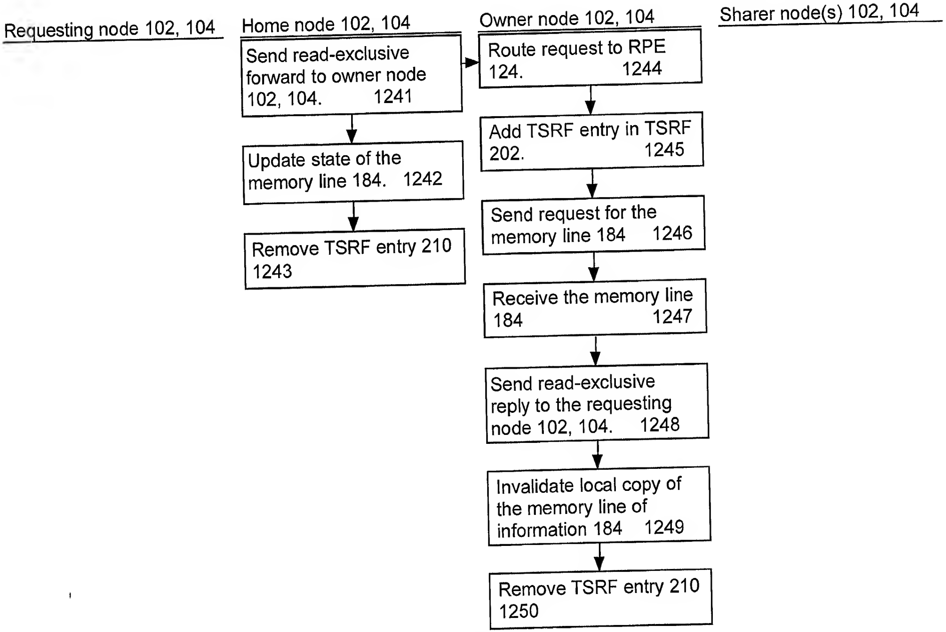

Requesting node 102, 104
Home node 102, 104
Owner node 102, 104
Sharer node(s) 102, 104
Send read-exclusive forward to owner node 102, 104. 1241
Update state of the memory line 184. 1242
Remove TSRF entry 210 1243
Route request to RPE 124. 1244
Add TSRF entry in TSRF 202. 1245
Send request for the memory line 184 1246
Receive the memory line 184 1247
Send read-exclusive reply to the requesting node 102, 104. 1248
Invalidate local copy of the memory line of information 184 1249
Remove TSRF entry 210 1250

Figure 12D

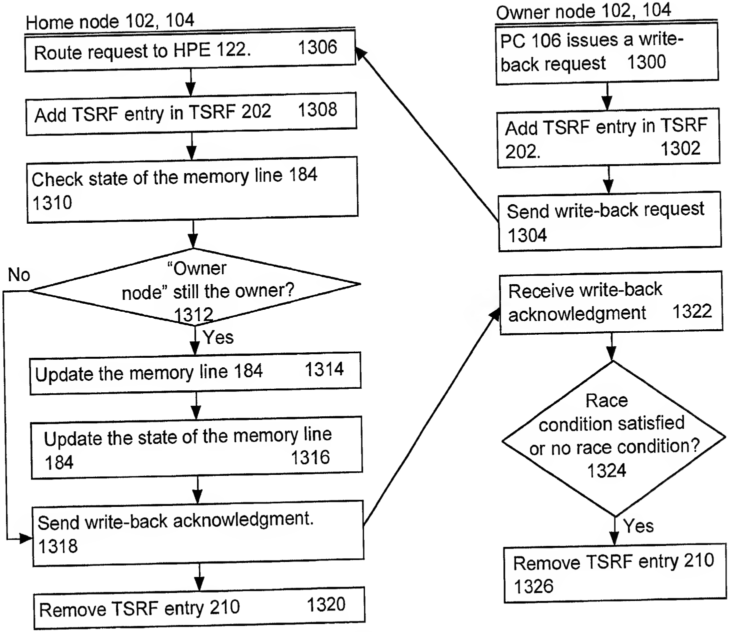

Home node 102, 104
Route request to HPE 122. 1306
Add TSRF entry in TSRF 202 1308
Check state of the memory line 184 1310
"Owner node" still the owner? 1312
No
Yes
Update the memory line 184 1314
Update the state of the memory line 184 1316
Send write-back acknowledgment. 1318
Remove TSRF entry 210 1320
Owner node 102, 104
PC 106 issues a write-back request 1300
Add TSRF entry in TSRF 202. 1302
Send write-back request 1304
Receive write-back acknowledgment 1322
Race condition satisfied or no race condition? 1324
Yes
Remove TSRF entry 210 1326

Figure 13

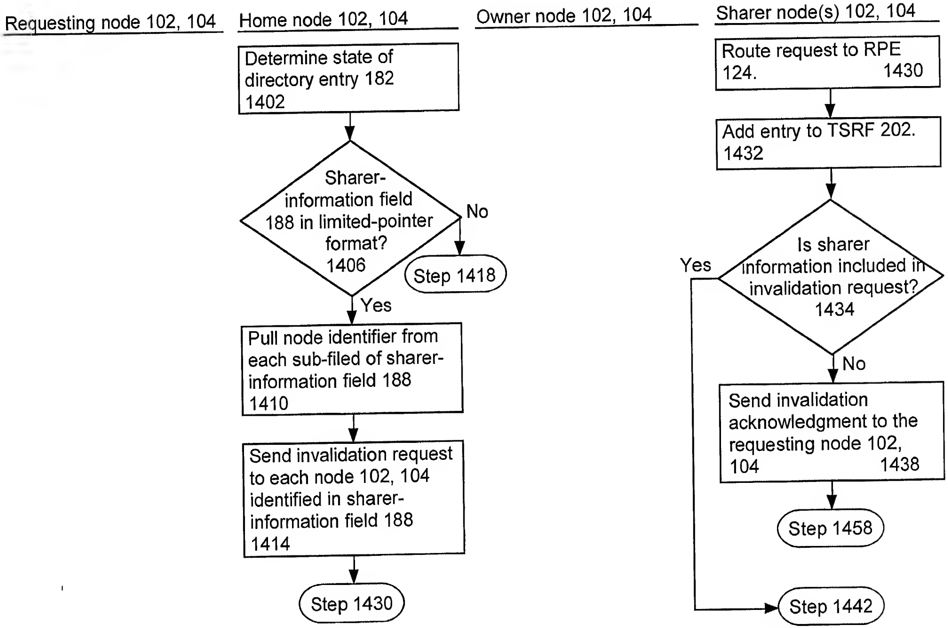

Requesting node 102, 104
Home node 102, 104
Owner node 102, 104
Sharer node(s) 102, 104
Determine state of directory entry 182 1402
Sharer-information field 188 in limited-pointer format? 1406
No
Step 1418
Yes
Pull node identifier from each sub-filed of sharer-information field 188 1410
Send invalidation request to each node 102, 104 identified in sharer-information field 188 1414
Step 1430
Route request to RPE 124. 1430
Add entry to TSRF 202. 1432
Is sharer information included in invalidation request? 1434
Yes
No
Send invalidation acknowledgment to the requesting node 102, 104 1438
Step 1458
Step 1442

Figure 14A

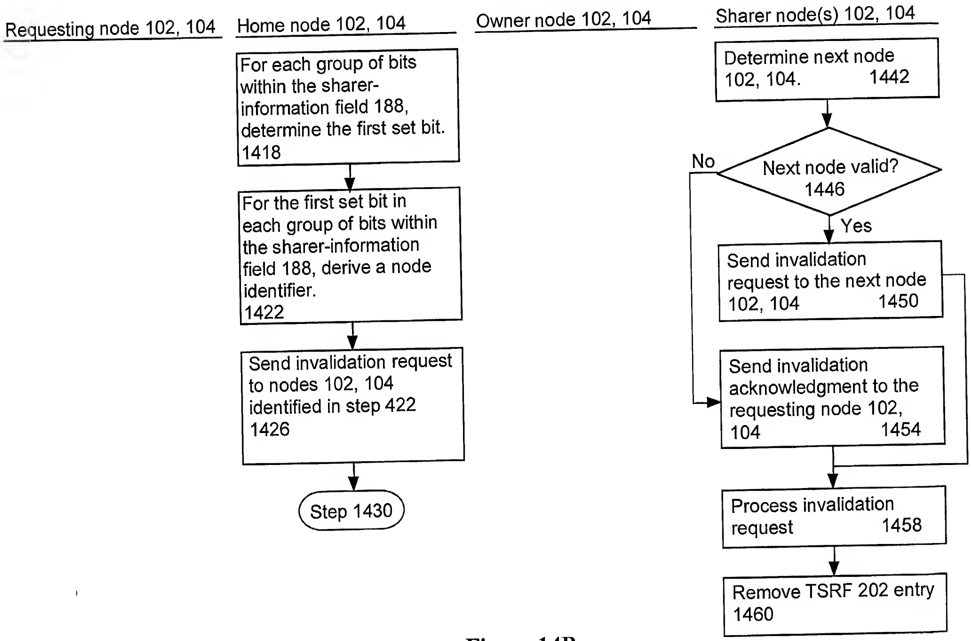

Requesting node 102, 104
Home node 102, 104
Owner node 102, 104
Sharer node(s) 102, 104
For each group of bits within the sharer-information field 188, determine the first set bit. 1418
For the first set bit in each group of bits within the sharer-information field 188, derive a node identifier. 1422
Send invalidation request to nodes 102, 104 identified in step 422 1426
Step 1430
Determine next node 102, 104. 1442
Next node valid? 1446
No
Yes
Send invalidation request to the next node 102, 104 1450
Send invalidation acknowledgment to the requesting node 102, 104 1454
Process invalidation request 1458
Remove TSRF 202 entry 1460

Figure 14B

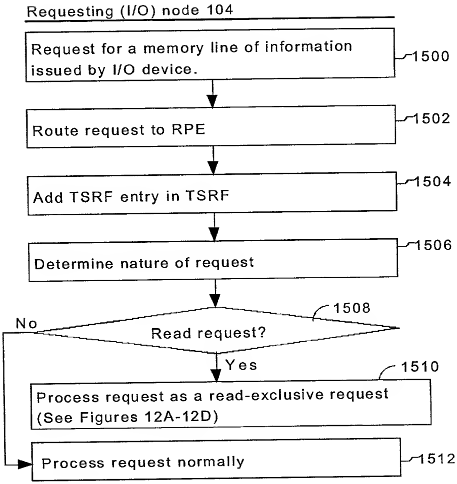


Figure 15

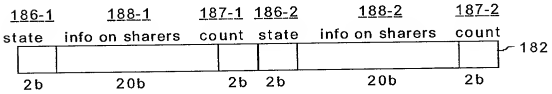
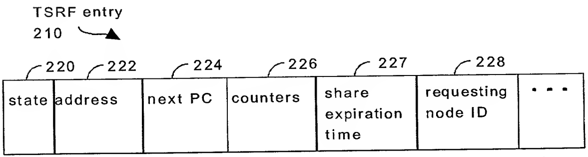


Figure 17



TSRF entry format

Figure 18

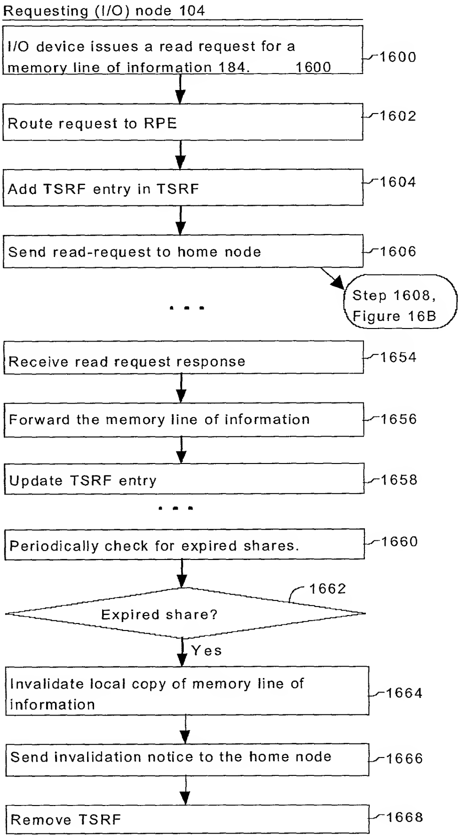

Requesting (I/O) node 104
I/O device issues a read request for a memory line of information 184. 1600
1600
Route request to RPE
1602
Add TSRF entry in TSRF
1604
Send read-request to home node
1606
Step 1608, Figure 16B
Receive read request response
1654
Forward the memory line of information
1656
Update TSRF entry
1658
Periodically check for expired shares.
1660
Expired share?
1662
Yes
Invalidate local copy of memory line of information
1664
Send invalidation notice to the home node
1666
Remove TSRF
1668

Figure 16A

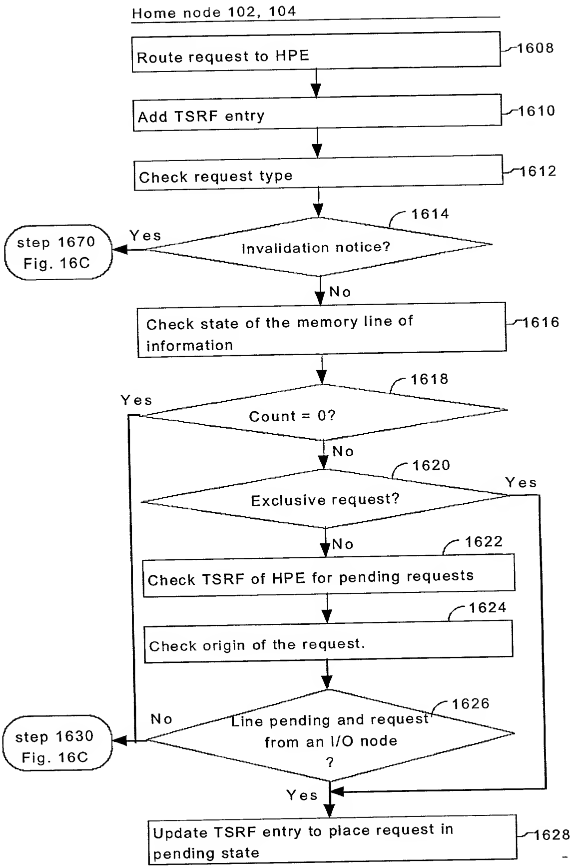

Home node 102, 104
Route request to HPE
1608
Add TSRF entry
1610
Check request type
1612
1614
Invalidation notice?
Yes
step 1670
Fig. 16C
No
Check state of the memory line of information
1616
1618
Count = 0?
Yes
No
1620
Exclusive request?
Yes
No
1622
Check TSRF of HPE for pending requests
1624
Check origin of the request.
1626
Line pending and request from an I/O node ?
No
step 1630
Fig. 16C
Yes
Update TSRF entry to place request in pending state
1628

Figure 16B

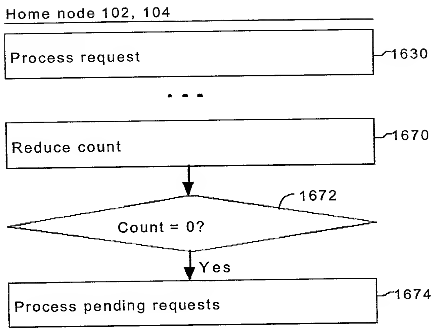

Home node 102, 104
Process request
1630
Reduce count
1670
1672
Count = 0?
Yes
Process pending requests
1674

Figure 16C